In the Claims:

1. – 4. (Canceled).

5. (Currently Amended). A receiver baseband apparatus, comprising:

an input unit adapted to receive an I and Q signal;

a first matched filter adapted to receive said I signal and generate an I filtered output therefrom;

a second matched filter adapted to receive said Q signal and generate a Q filtered output therefrom;

a processor programmed to perform the steps of:

detecting the presence of signal activity as input to said receiver baseband apparatus;

acquiring said signal activity by performing coarse phase acquisition on said signal activity once it is detected, wherein said performing coarse phase acquisition comprises:

rotating vectors z_n representing said signal activity into a single quadrant by an angle Θk;

wiping off said $z_n(\Theta k)$ modulation;

summing the wiped off vectors $z_n(\Theta k)$;

determining the energy contained within a plurality of hypotheses; and

selecting a single hypothesis from said plurality of hypotheses having the maximum energy;

pre-tracking said signal activity once it is detected; and

tracking said signal activity once it is detected;

a decoder adapted to receive said I filtered output signal and said Q filtered output signal from said processor and to generate a decoded output therefrom;

a deinterleaver adapted to generate a deinterleaved output in accordance with said decoded output signal input thereto;

a forward error correction decoder adapted to generate output receive data in accordance with said deinterleaved output signal input thereto; and

a controller adapted to manage and control said input unit, first matched filter, second matched filter, said processor, said decoder, said deinterleaver and said forward error correction decoder.

6. – 10. (Canceled).

11. (Currently Amended). A receiver baseband apparatus, comprising:

an input unit adapted to receive an I and Q signal;

an I matched filter adapted to receive said I signal and generate an I filtered output therefrom;

a Q matched filter adapted to receive said Q signal and generate a Q filtered output therefrom;

a processor programmed to:

perform automatic gain control (AGC) and generate an AG control signal therefrom;

perform timing detection and generate an analog to digital (A/D) clock control signal therefrom;

perform phase detection and generate a voltage controlled oscillator (~~CVO~~ VCO) control signal therefrom;

a decoder adapted to receive said I filtered output signal and said Q filtered output signal from said processor and to generate a decoded output therefrom;

a deinterleaver adapted to generate a deinterleaved output in accordance with said decoded output signal input thereto;

a forward error correction decoder adapted to generate output receive data in accordance with said deinterleaved output signal input thereto; and

a controller adapted to manage and control said input unit, I matched filter, Q matched filter, said processor, said decoder, said deinterleaver and said forward error correction decoder.

wherein said processor is further operable to acquire signal activity by performing coarse phase acquisition on said signal activity, wherein said performing coarse phase acquisition comprises:

rotating vectors z_n representing said signal activity into a single quadrant by an angle Θk;

wiping off said $z_n(\Theta k)$ modulation;

summing the wiped off vectors $z_n(\Theta k)$;

determining the energy contained within a plurality of hypotheses; and

selecting a single hypothesis from said plurality of hypotheses having the maximum energy.

12. – 15 (Canceled).

16. (Currently Amended). The apparatus according to claim 11, wherein said processor is further operable to pre-track said signal activity by performing timing

acquisition on K groups, each made up of N DFT estimates, each estimate calculated from blocks of 16 symbols, said performing timing acquisition comprising:

calculating a timing estimate t_i based on a DFT for 16 contiguous symbols, i=1,..,N,

thereby obtaining N DFT estimates each based on a block of symbols;

generating a histogram of said N DFT estimates t_i;

classifying a timing range said group the N estimates are in based on said histogram;

unwrapping said N DFT estimates and calculating their average T_i; and

unwrapping K average estimates T_i and performing a least square fit of said K averages so as to generate a final estimate.